PreLab 5 – Audio Speaker Driver

• GOAL

The goal of Lab 4 is to demonstrate a two audio amplifier. In PreLab 4 you will investigate a emitter followers and Darlington pair transistors.

• DARLINGTON FOLLOWER

It is a bad idea to connect an audio speaker to a common emitter amplifier, because the speaker impedance (e.g. 16 ohm) is MUCH lower than the common emitter's output impedance (> 1 kohm). You will get almost no output at all! ☹

An emitter follower obviously helps, but we need extra large β to deal with the very low speaker impedance. Darlington to the rescue! Using TWO transistors in series provides a total current gain of about 10,000. Nice! ☺

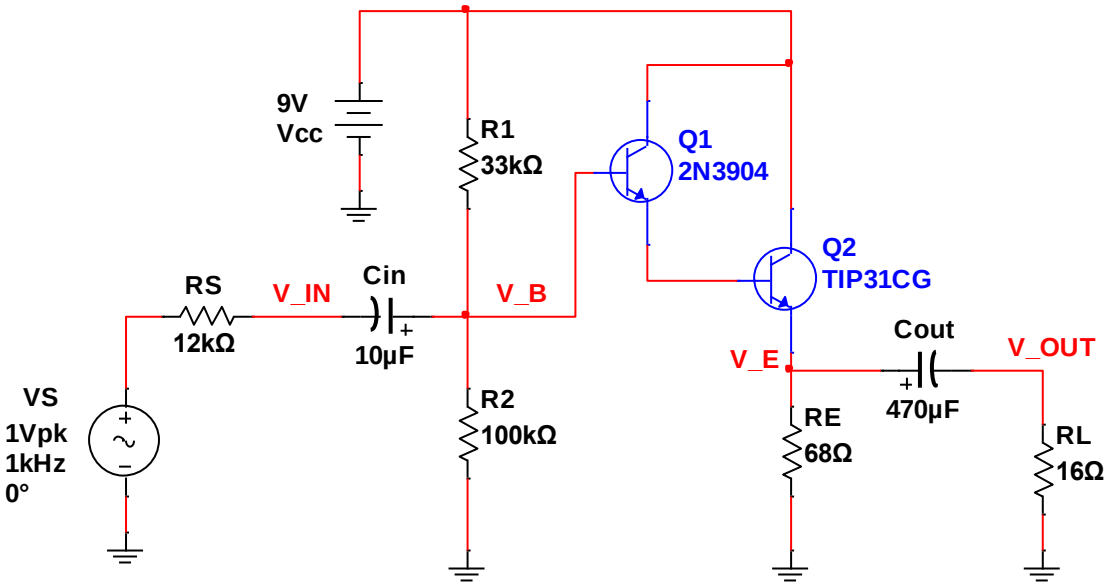

Fig. 1: Darlington follower acts as a voltage buffer between the signal source and low impedance load.

- **TASK 1**: Enter the circuit schematic for the Darlington follower shown in Fig. 1 in Multisim.
  - The Darlington connection is made with the 2N3904 and TIP31C transistors.
  - VS is an AC voltage source (sine wave, 1 Vpeak, 1 kHz).
    - The 12 kohm resistor is intended to mimic the output impedance of the Lab 3 common emitter.
  - We'll model the speaker as a 16 ohm resistor (this is not a good model, but is OK for now).
  - Properly label the net names for V_IN, V_B, V_E, and V_OUT.

- **TASK 2**: Perform a DC Operating Point Analysis:
  - Fill out Table 1 with your simulated values for V_B and V_E.
  - Calculate (e.g. by hand) the theoretical values for V_B and V_E.
    - Is the voltage divider stiff? If not, use KVL to determine V_B.
    - Assume V_BE= 0.7V and beta = 100 for both transistors. Show all work!

Table I: DC Operating Point Analysis

Simulation		Theory	
V_B	V_E	V_B	V_E

- **TASK 3**: Perform a Transient Analysis:
  - Use simulation start and stop times of TSTART = 0 and TSTOP = 2 ms, respectively.
  - **Submit a plot showing both V_IN and V_OUT together.**
  - Measure the peak-to-peak values for V_IN and V_OUT and compute the resulting amplifier gain.
  - Compute the theoretical voltage gain using $A = r_e / (r_e' + r_e)$. Assume $\beta = 100$ and $V_{BE} = 0.7$ for both transistors. Show all work.
  - Compute the theoretical input and output impedance (e.g. using formulas from lecture).
  - Complete Table 2 with your measured and theoretical values.

Table II: Transient Analysis

V_IN (pp, sim)	V_OUT (pp, sim)	Gain (sim)	Gain (theory)	Z_IN (theory)	Z_OUT (theory)

- **TASK 4**: OK! Now it's time to analyze your simulation results to see if they make sense! Answer the following:
  - A good voltage buffer should have $V_{OUT}/V_{IN} > 0.9$. Is this the case for the simulated Darlington follower?
  - The output impedance Z_{OUT} of a buffer should be at least 10 times smaller than the load R_L. Does your theoretical Z_{OUT} satisfy this criterion?

➢ **Make sure you submit the following**:
  - Circuit schematic and plot showing V_IN and V_OUT together.
  - Completed Table 1 and 2. Include all work for theoretical calculations.
  - Answers to the TASK 3 questions.

(End of PreLab 4)