ECE 318/518
CSC 318/518
Digital Design

Syllabus

Catalog Description

This course builds on the introductory material of ECE118. Students are already familiar with the fundamental principles and devices used in digital logic and in this course the emphasis is on the design of more complex digital systems. VHDL will be learned and used extensively throughout the course as this is one of the two most commonly used hardware design languages in industry. The theory learned in the lectures will be put into practice in a series of laboratories which complement the lecture material. At the end of the course, each student will choose a design project to work on during the last few weeks.

Prerequisites

ECE118 is a prerequisite for this course and is taken by all EE and CpE students in their second year.

Writing Across the Curriculum (WAC)

In this course there is a significant writing component which comprises 5 laboratory reports as well as a final design report. The course is designated as a WAC course and students laboratory and project reports will be partially graded on the quality of the technical writing in these reports.

Objectives and Outcomes

At the completion of this course, successful students will be able to:

- Use VHDL to describe combinational and sequential logic, finite state machines
- Design hazard-free combinational circuits and analyze sequential circuit timing
- Develop simulation inputs for digital hardware designs and develop a test plan for their digital design
- Present a well-organized laboratory report

A more comprehensive list of the objectives of this course is available at the course web site address: http://logopolis.union.edu/ece318/ece318index.html

Outcome Measures and Assessment

Progress and final outcomes will be measured using the following indicators:

- weekly homework exercises that demonstrate understanding of the material covered in lectures
- laboratory reports on practical topics that reinforce and extend concepts learned in class
- midterm and final in-class exams that measure individual understanding of lecture material and laboratory work
- a project of the student's choosing which will test the student's ability to take a design from the initial design phase all the way through to the testing of the project synthesized in hardware
- laboratory reports and a final project report which test technical writing proficiency

Course Website

The URL for the course website is: http://logopolis.union.edu/ece318/ece318index.html

Course Details

Instructor: Professor Hedrick
Email: hedrickj@union.edu
Phone: (518) 388-8027
Office: 223 Steinmetz Hall

Class Times: Tuesday, Thursday 10:55 to 12:40 in NWSE 106
Laboratory Time: Tuesday 1:55 to 4:45 in NWSE 106

Required Text

These two texts are required for the course:

- "Digital Systems Design with VHDL" by Mark Zwoliński, Prentice Hall, 2nd Edition, 2004, ISBN 0-13-039985-X
- "Rapid Prototyping of Digital Systems, A Tutorial Approach", James O. Hamblen, Michael D. Furman, SOPC Edition, Kluwer Academic Publishers, 2008, ISBN 978-0-387-72670-0

Homework assignments will be given on a Thursday and are due on the following Thursday. 20% will be deducted **per day** for late assignments.

Each student should work on the homework problems individually. Copying of other's homework will not be tolerated. Homeworks are graded on both effort and results. It is important that you see your instructor for additional explanation if you have problems doing the homework.

Laboratories

Each student will complete 5 laboratories as well as a design project. For each of these exercises, the student will be expected to write a laboratory report. 50% of the grade for the lab will be given for attendance and willingness to learn in the lab. The other 50% will be based on the report. The report is due at the next laboratory. 20% will be deducted **per day** for late assignments. The guidelines for writing the laboratory report are available at the course web site.

Exams

There will be one midterm exam in the 6^{th} or 7^{th} week.

The final will be two hours long and be cumulative (i.e. include questions from each part of the course). The final exam date and time will be announced once the registrar decides on it.

Grading

Grades are based on weekly homeworks, a midterm exam, a final exam, laboratory reports and a design project.

Final Exam	35%
Midterm Exam	20%
Homework	15%
Labs	15%
Project	15%

Cheating/Plagiarism

Cheating on a test or homework will be handled according to the Union College's academic code of conduct and policies. Both the person who copies the work and the person the work is copied from may be held equally responsible.

Disability

If you have or believe you have a disability, it is your responsibility to inform me in a timely manner if services/accommodations provided are not meeting your needs.

Religious Holidays

I will try not to schedule exams during a religious holiday but there are a lot of religions so let me know if you will be away and I will do my best to accommodate you with homework and exams.

Course Outline

This is a rough outline of the course:

Weeks 1-5: Review of ECE118 material, VHDL design of combinational logic, VHDL design of sequential logic, latches and flip-flops, registers, counters, algorithmic state machines and synthesis from ASM charts **[Midterm exam will be in week 6/7]**

Weeks 6-10: Memory, CPLDs and FPGAs, complex sequential systems, datapath/controller partitioning, VHDL simulation and synthesis, system design [**Final Exam during Exam Week]**

A more detailed outline of the course material with a weekly outline of the topics covered is online at the course web site.
The schedule is approximate and we may take more or less time on a topic as we require. The midterm exam date will be set at least a week before. All exams will be based on the lecture material, homework and laboratories.

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