HW #2
Due Date: Thursday January 24th at 10.30 a.m.

Note: submit both the code and the simulation output for each problem requiring simulation

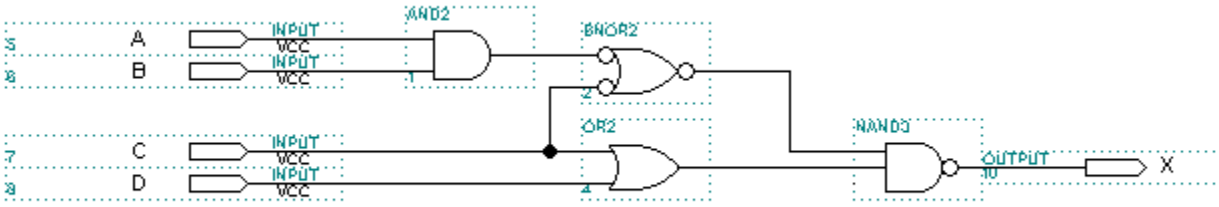
1. Read chapters 3 and 4 in the Zwolinski textbook.

2. Write a VHDL model that uses concurrent signal assignments (without delays, i.e., no "after" required) to model the following circuit. Find the maximum delays using the timing analyzer in Quartus for the following devices:

a) Max 7000S family, device EPM7128SLC84-15

b) Flex 10K family, device EPF10K70RC240-4

c) Cyclone II family EP2C35F672C6



3. The following VHDL program is a structural description of a circuit that uses NOR2, AND2 and NOT components. In the port map statements the output signal is the last signal. Draw the circuit that is described and give the function table for the circuit.

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY mystery_ckt IS
 PORT(
  D, C   : IN STD_LOGIC;
  Q, Q_b : OUT STD_LOGIC);
END mystery_ckt;

ARCHITECTURE structural OF mystery_ckt IS
 SIGNAL R, S, D_b : STD_LOGIC;
BEGIN
AND_1: AND2 port map (D, C, S);
AND_2: AND2 port map (C, D_b, R);
NOT_1: NOT port map (D, D_b);
NOR_1: NOR2 port map (S, Q, Q_b);
```

```
NOR_2: NOR2 port map (Q_b, R, Q);
END structural;
```

4. Write a VHDL description of a full-adder that uses conditional assignment statements (***when-else***). Simulate the VHDL model (in Quartus or ModelSim) to verify that it works correctly.

5. Write a VHDL description of a 2 to 4 decoder with active low outputs and an enable input that uses conditional assignment statements (***when-else***). When the decoder is disabled, the outputs should all be inactive (high). Simulate the VHDL model (in Quartus or ModelSim) to verify that it works correctly.

6. Repeat the active low decoder design of problem 4, but use a selected assignment statement (***with-select***). Simulate the VHDL model (in Quartus or ModelSim) to verify that it works correctly.