HW #3
Due Date: January 30th at 10.30a.m.

Note: submit both the code and the simulation output for each problem requiring simulation

1. Write a VHDL model that uses concurrent signal assignments to model the circuit in Figure 1. Use the "after" clause to model the delays accurately. The NAND gates have a delay of 4ns and the inverters have a delay of 2ns. Hint: You will need to define internal signals. **Simulate the circuit in ModelSim** for the following input cases to illustrate that the delays are modeled properly. ABCD= 0001, 1111, 1101. To simplify the simulation, here are some commands you can use in the simulator rather than creating a testbench:

VSIM> force A 0; force B 0; force C 0; force D 1
VSIM> run
VSIM> force A 1; force B 1; force C 1; force D 1
VSIM> run
VSIM> force A 1; force B 1; force C 0; force D 1
VSIM> run

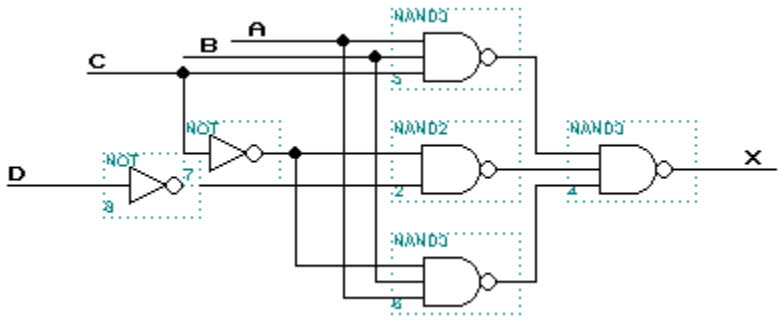

Figure 1

2. Given the following VHDL process, write a conditional dataflow signal assignment statement (i.e., using when … else) that does the same thing.

```
process (a, b)
begin
    if a = '1' then
        cout <= "001";
    elsif b = '1' then
        cout <= "010";
    else
        cout <= "100";
    end if;
end process;
```

3. The "–" in the truth table is a "don't care".

A(2 downto 0)			F(1 downto 0)
0	0	0	00
0	0	1	01
0	1	–	10
1	–	–	11

a. Write a conditional signal assigment (when … else) that models the function.
b. Write a selected (select … when) signal assignment that models the function.

4. Analyze the following VHDL program and describe what it does. Be sure to describe both timing and function. [Note: you may want to do a simulation to help you understand the code.]

```
library ieee;
use ieee.std_logic_1164.all;

entity hw3_6 is
port (reset, clk: in std_logic;
         F: buffer std_logic_vector(3 downto 0));
end hw3_6;

architecture hw_3 of hw3_6 is
begin
process(clk)
             variable C: std_logic_vector(3 downto 0);
             begin
                C := F;
                  if clk = '0' then
                     if reset = '1' then
                        C := "0000";
                     else
                        for i in 0 to 3 loop
                          if C(i) = '1' then
                                C(i) := '0';
                          else
                                C(i) := '1';
                                exit;
                          end if;
                        end loop;
                    end if;
                  end if;
                F <= C;
end process;
end hw_3;
```

5.

a. Find the state table for the following VHDL model of a finite state machine.

b. Write down logic expressions which could be used as flip-flop inputs to determine the transitions to the next state (you may need to review your state machines from ECE118 to complete this part).

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;


ENTITY fsm3 IS
PORT( x, clk, reset:  IN  STD_LOGIC;
              state: BUFFER STD_LOGIC_VECTOR(1 downto 0);
                  z:  OUT STD_LOGIC);
END fsm3;

ARCHITECTURE synthesis OF fsm3 IS
  SIGNAL state_input: STD_LOGIC_VECTOR(2 downto 0);
  BEGIN

state_input <= state & x;

  PROCESS
  BEGIN
  WAIT UNTIL clk = '1';
  IF reset = '1' THEN
         state <= "00";
  ELSE
   CASE (state_input) IS
     WHEN "000" =>
   state <= "00";
     WHEN "001" =>
   state <= "01";
     WHEN "010" =>
   state <= "01";
     WHEN "011" =>
   state <= "10";
     WHEN "100" =>
   state <= "10";
     WHEN "101" =>
   state <= "00";
     WHEN OTHERS => null;
   END CASE;
  END IF;
END PROCESS;

z <= NOT (state(0) OR state(1));

END synthesis;
```

6. The flip-flop in the circuit in Figure 2 has a propagation delay from clock edge to Q of 2 ns. Its setup time is 1 ns and hold time is .5ns.

a. If the maximum clock speed of this circuit is 166 MHz, what is the maximum delay of the combinational logic from Q to D?

b. If the NOR and NAND gates have equal gate delays, what is the delay of these gates?

c. Is this a Mealy or Moore finite state machine?

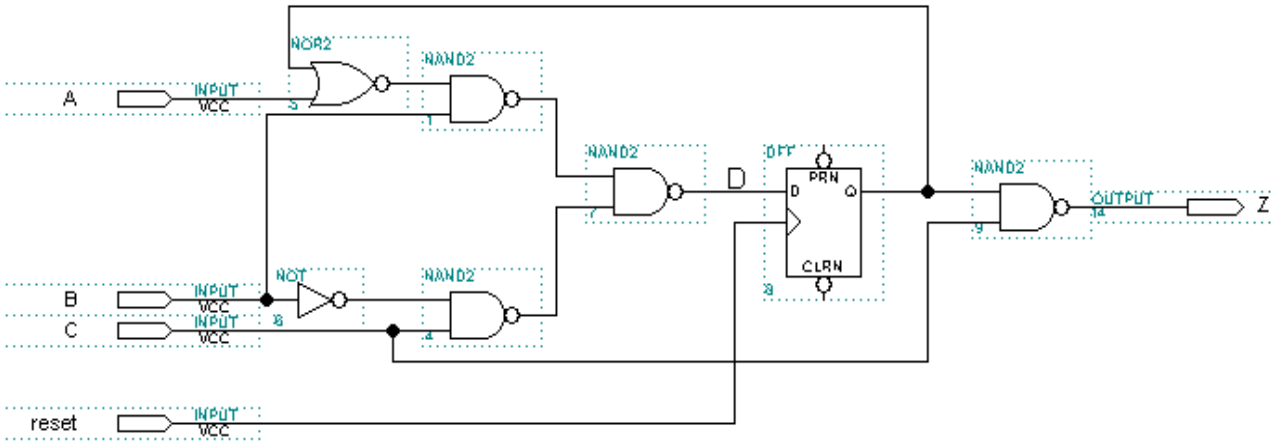

Figure 2

7.

a. For the circuit in Problem 6, give a timing diagram that illustrates the window of time when the inputs are allowed to change. You may assume that the inverter has 1/2 the delay of a NOR or NAND gate.

b. Is there a combinational hazard possible on line D?

c. If the answer to b was yes, would it cause incorrect operation of the finite state machine? Why or why not?

Winter 2013