Union College
ECE 318
Assignment 2 Solutions

Problem 2.

Code Listing:

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

ENTITY hw2_1 IS
 PORT(
  A,B,C,D  : IN STD_LOGIC;
  X : OUT STD_LOGIC);
END hw2_1;


ARCHITECTURE data_flow OF hw2_1 IS
 SIGNAL AB, CD, ABC: STD_LOGIC; -- internal signals in the circuit
BEGIN
AB <= A AND B;
CD <= C OR D;
ABC <= (NOT C) NOR (NOT AB);
X <= CD NAND ABC;
END data_flow;
```

Results:

EPM7128SLC84-15

Actual P2P Time	From	To
15.000 ns	C	X
15.000 ns	A	X
15.000 ns	B	X

EPF10K70RC240-4

Actual P2P Time	From	To
19.100 ns	C	X
19.100 ns	B	X
18.800 ns	A	X

EPM7128SLC84-7

Actual P2P Time	From	To
7.500 ns	C	X
7.500 ns	A	X
7.500 ns	B	X

Problem 3.

This is a (clocked) D latch circuit. See the figure below

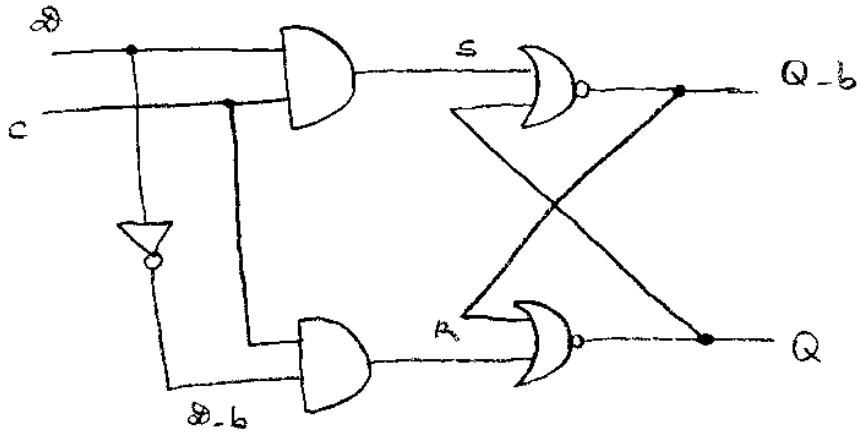

Figure 1. Circuit diagram described by code in Q2

Problem 4.

Code Listing:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

    ENTITY fulladder IS
        PORT(
            Ain:  IN STD_LOGIC;
            Bin:  IN STD_LOGIC;
            Cin:  IN STD_LOGIC;
           Cout:  OUT STD_LOGIC;
           Sout:  OUT STD_LOGIC);
    END fulladder;
```

```
ARCHITECTURE synthesis OF fulladder IS

BEGIN

    Sout <= '1' when (A xor B xor Cin) = '1' else
            '0';

     Cout <= '1' when ((A and B) or (A and Cin) or (B and Cin)) = '1' else
            '0';

END synthesis;
```

Simulation:

The simulation results are shown in figure 2:

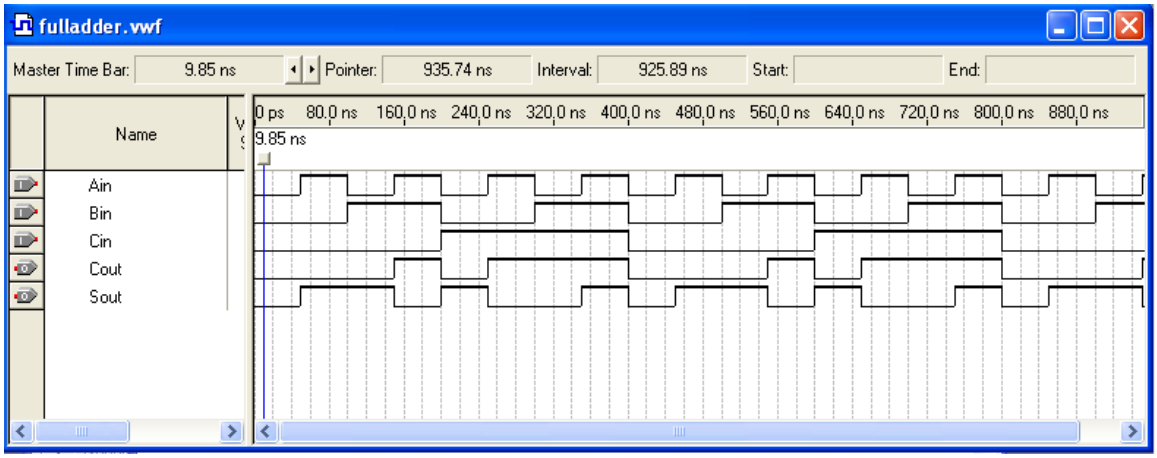

Figure 2. Simulation results for Q3

Problem 5.

Code Listing:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

    ENTITY decoder IS
        PORT(
            S:  IN STD_LOGIC_VECTOR(1 downto 0);
            en:  IN STD_LOGIC;
            Dout:  OUT STD_LOGIC_VECTOR(3 downto 0));
    END decoder;
```

```
ARCHITECTURE when_else OF decoder IS

BEGIN

    Dout <= "1111" when en = '0' else
                "0111" when S = "11" else
                    "1011" when S = "10" else
                    "1101" when S = "01" else
                    "1110" when S = "00" else
                    "XXXX";

END when_else;
```

Simulation:

The simulation results are shown in Figure 3.

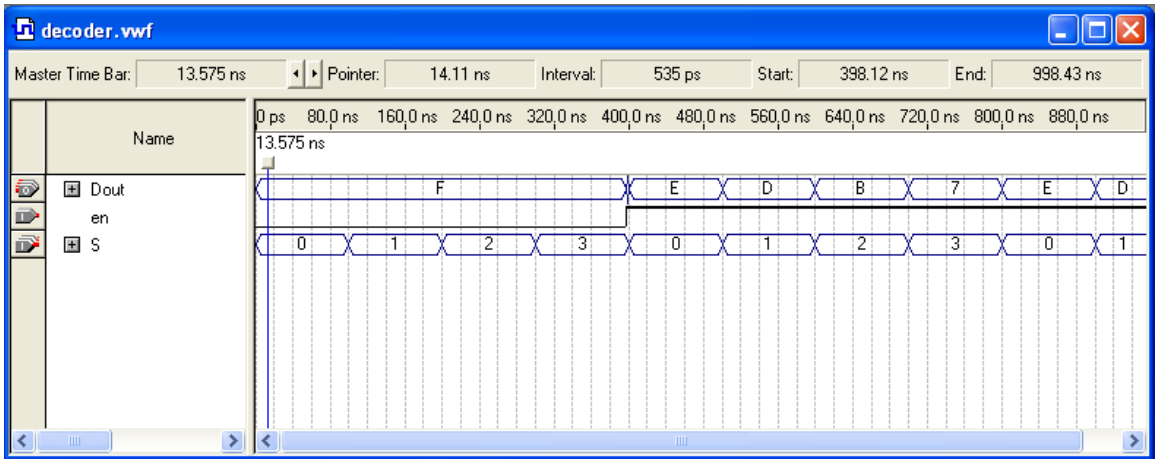

Figure 3. Simulation results for Q4.

Problem 6.

Code Listing:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY decoder2 IS
    PORT(
        S:  IN STD_LOGIC_VECTOR(1 downto 0);
       en:  IN STD_LOGIC;
      Dout:  OUT STD_LOGIC_VECTOR(3 downto 0));
END decoder2;
```

```
ARCHITECTURE with_select OF decoder3 IS
        SIGNAL SEL: STD_LOGIC_VECTOR(2 downto 0);
   BEGIN
        SEL(0) <= en;
        SEL (2 downto 1) <= S;
        WITH SEL SELECT
       Dout <=          "1111" when "000" | "010" | "100" | "110",
                        "0111" when "111",
                              "1011" when "101",
                              "1101" when "011",
                              "1110" when "001",
                              "XXXX" when others;

END with_select;
```

Simulation:

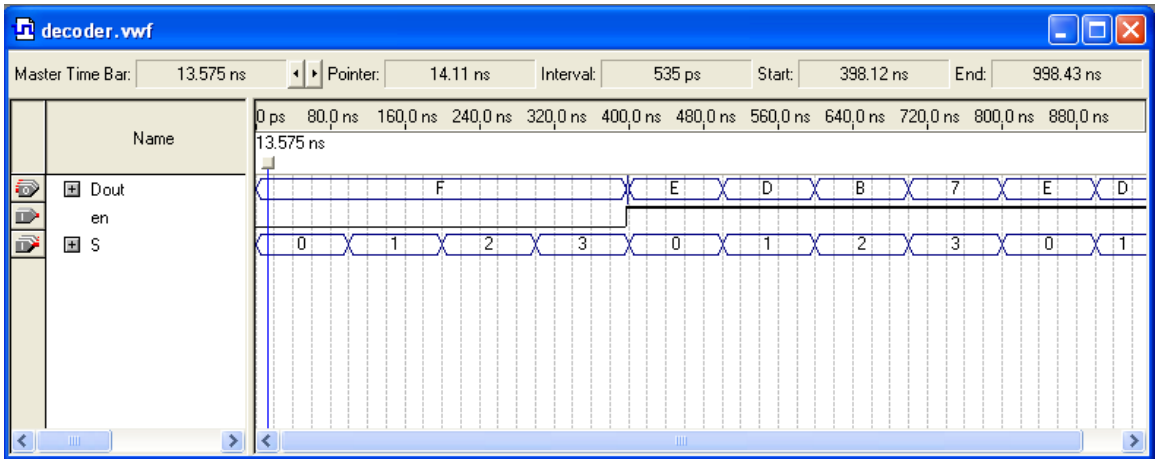

Figure 4. Simulation results for problem 5

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