ECE318 Laboratory #1
Lab Date: Jan. 15th Report Due: Jan. 20th

Introduction to Altera Quartus II: Schematic Entry, VHDL, and Hazards

1. Introduction

In this lab, we will start by entering a simple circuit as a schematic file (you may recall doing this in ECE118). We will then compile the circuit and simulate its behavior. We will download our design to the CPLD board and test the design on the hardware itself. We will examine timing and the placement of the design on the board. We will carry out some simple modifications to the original design to increase our understanding of the Quartus II software. In this course we will be using the SOPC Edition of the "Rapid Prototyping of Digital Systems" textbook and version 9.1 sp2 Web Edition of the Quartus II software.

2. Prelab

Read through chapters 1 and 2 of "Rapid Prototyping of Digital Systems – SOPC Edition" (we will refer to this as the lab text). This laboratory will be based on chapter 1 of the text and chapter 2 gives a good overview of the board which we will be using in lab. Note that we will be using the Altera DE2 development board.

3. Procedure

A. Setup the Quartus II software for your account

We will first customize our view by going to "Tools – Customize". Make sure that the Quartus II option is checked under "Look and Feel". Then, click on the "Toolbars" tab and check off the toolbars shown in Figure 1 on the toolbars options. This will allow us to click on buttons instead of searching through menu items. I recommend these two items but you can change this later if you wish.

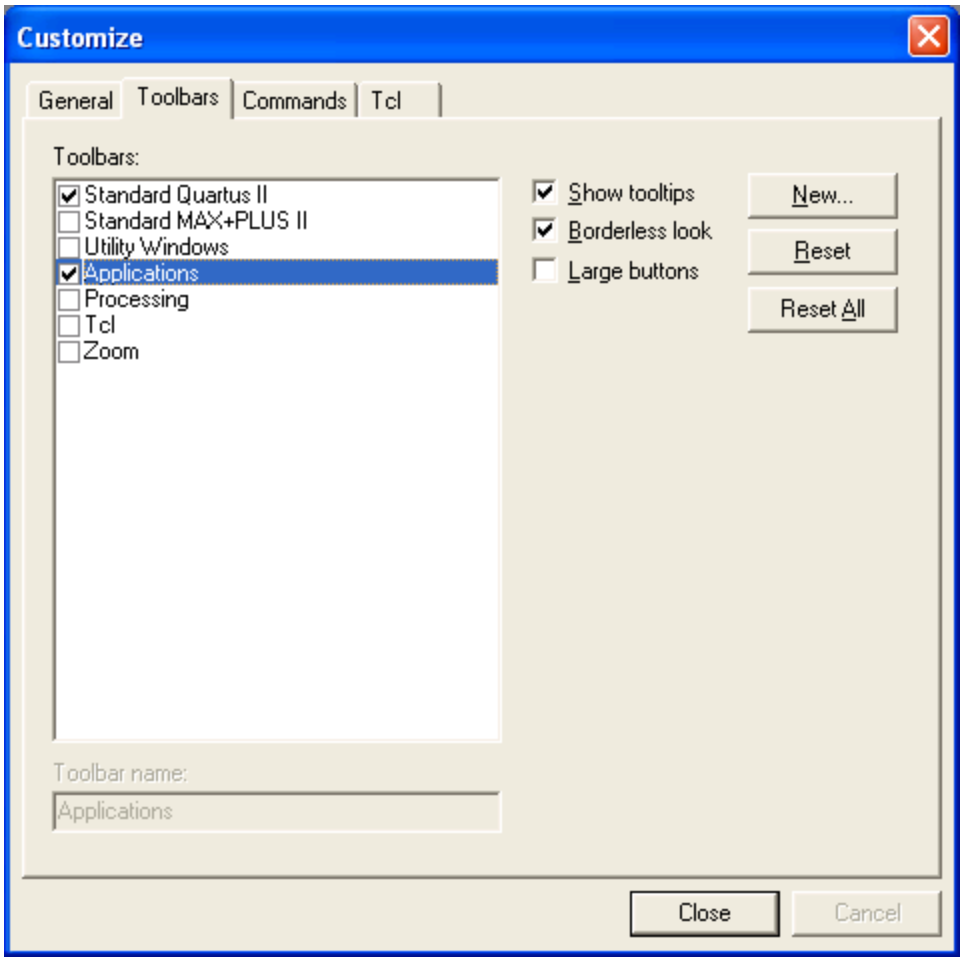

Figure 1. Toolbar options

B. Enter the circuit as a block diagram.

Open a new file by using "File – New" and then choose the type of file as "Block Diagram / Schematic File" as shown in Figure 2 below. We will follow the text and create the circuit shown in figure 1.12, page 14 of the lab text.

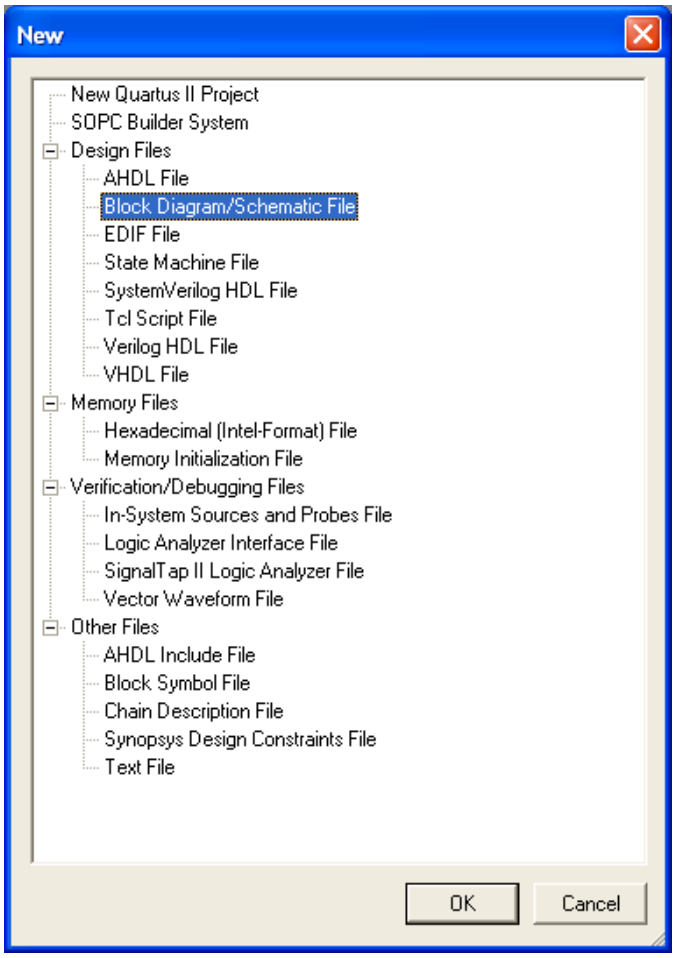

Figure 2. New file types

Enter the gate by clicking on the  **button symbol. This will give the listing shown in**

and then expand the libraries list and then expand the primitives list to see all the gates under logic-primitives.

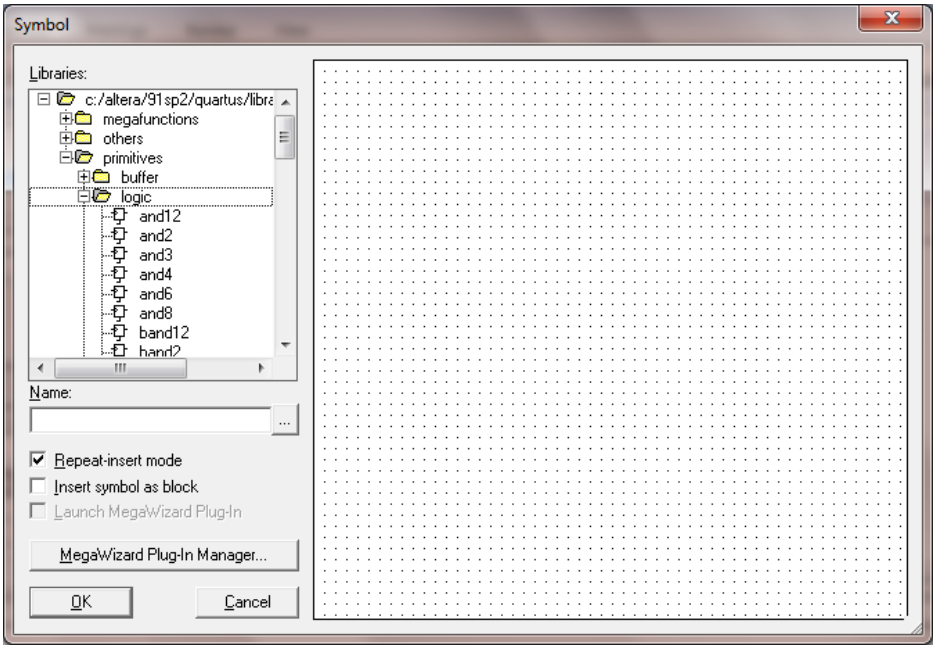

Figure 3. Logic blocks and gates

Enter the symbol bnor2 (which is bubbled NOR with 2 inputs). Next click on the  button to **save the file to a directory on your thumb drive (remember that all files are deleted on the local hard drive when you log out or the computer is rebooted)**. Something simple usually works best e.g., G:\ECE318\lab1\lab1.bdf. You will be prompted to start a new project and you should create one. A project is very similar to a folder where all the files associated with one task can be placed (see Figure 4).

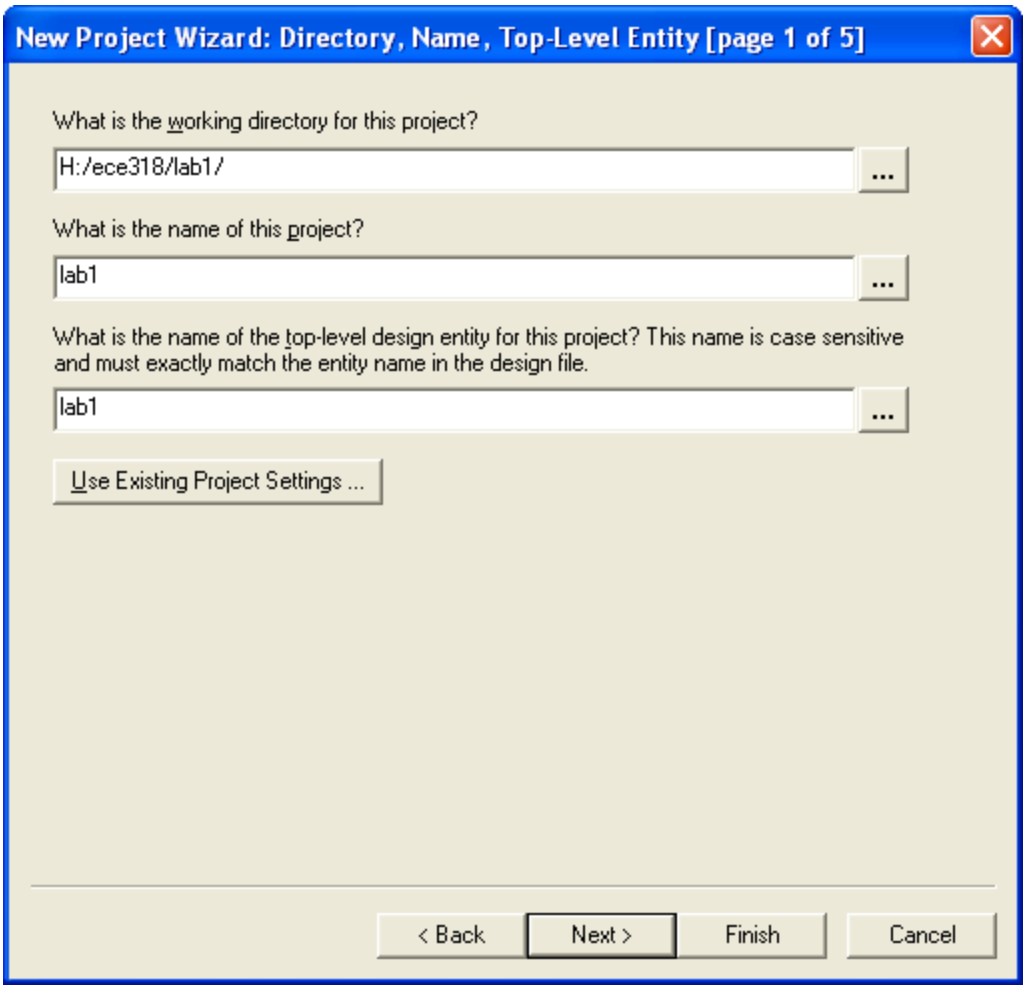

Figure 4. Creation of a new project - Step 1

You must keep the name of the project the same as the name of the design file (i.e., .bdf file which you have just created). Again, it is best to keep the names very simple. In particular, ensure that you do not have any spaces in your directory path or file name.

Click on "Next" to get to the third screen where we are asked to choose a device. Here we will choose the Cyclone II family and the EP2C35F672C6 device. You can check on the board that this is indeed our target device. (See **Error! Reference source not found.**.)

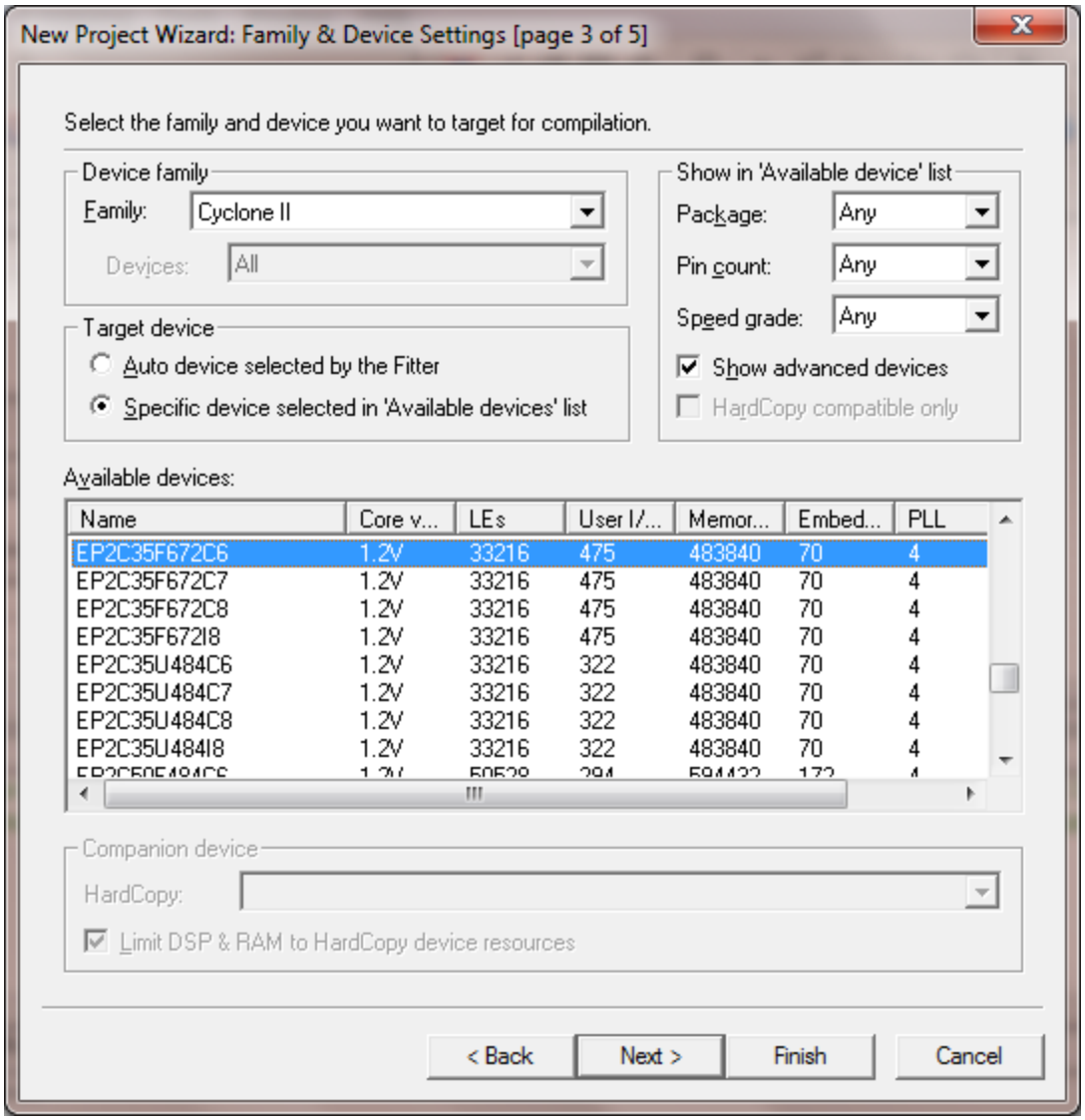

Figure 5. Choose a device - Step 3

Click on “Next” on page 4 and then on “Finish” on page 5.

C. Compilation and Pin Assignment

Follow the directions on pages 12 to the top of 16 of the text to enter the input and output pins and name them appropriately. Once you have completed this, compile the circuit using the instructions on page 16 of the text. You will get a warning “Warning: Feature LogicLock is only available with a valid subscription license. Please purchase a software subscription to gain full access to this feature.” This can be ignored. However, if you get an error (as opposed to a warning) then there is something amiss in your circuit.

If you get the pop-up shown in Figure 6. Below you can continue.

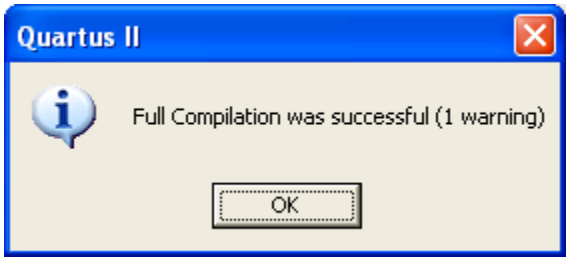

Figure 6. Compilation Successful

Now we will assign the inputs to certain pins on the physical device. Under "Assignments – Assignment Editor", we can set the input and output pins to correspond to pins on the actual physical device. Click on the location column and fill in the connections as given in Table 1.2 on page 14. Use the instructions found on pages 14 and 15 of the text to assign the correct pins. Your completed assignment should look like Figure 7. Save your work and compile the circuit again.

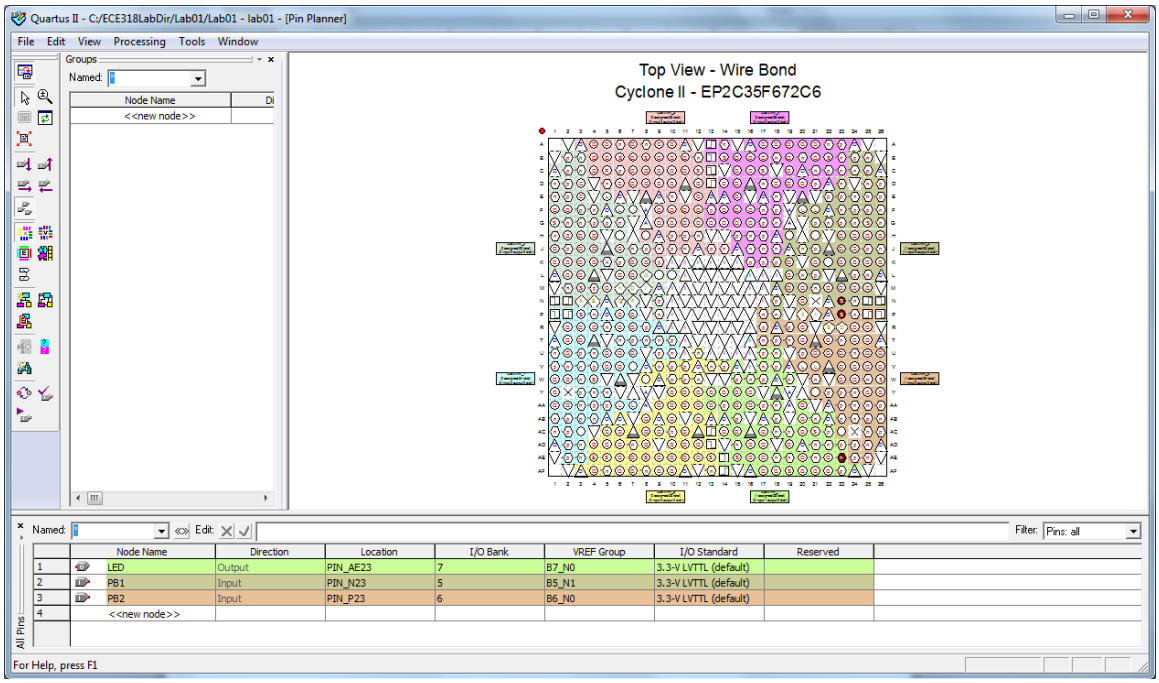

Figure 7. Assignment Editor

Once you complete the assignment your final circuit should be very similar to that shown in Figure 8.

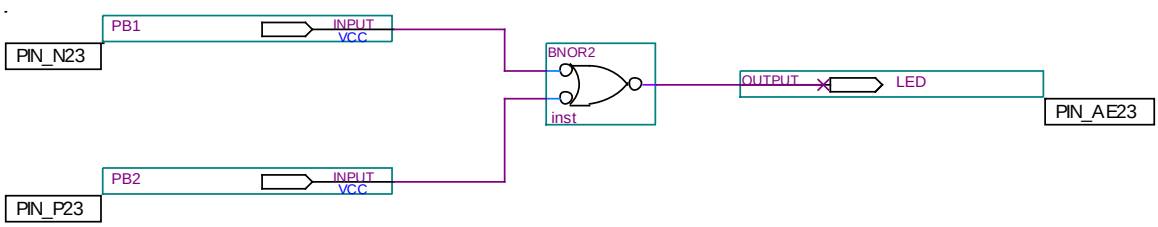

Figure 8. Completed circuit

D. Simulation

We are now ready to test the circuit. For larger projects this is best done in a simulation environment prior to downloading the design to the target board. We will carry out the simulation in this instance for illustrative purposes. Use the instructions on pages 17 and 18 in the textbook

First we will create a vector waveform file by clicking on "File – New" and selecting the appropriate file type (Figure 9).

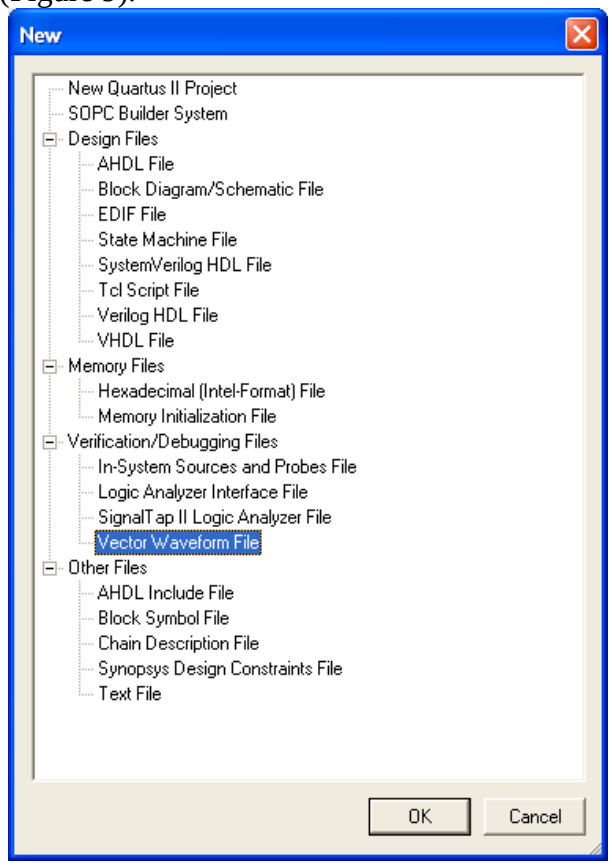

Figure 9. Creating a new simulation waveform file

By double clicking under “Name” and using “Node Finder”, we obtain all the input and output pins. Choose all the nodes as selected nodes and then click on “OK” (see Figure 10). We will now set the values of the inputs and find what the expected output will be. Follow the directions on page 11 of the text (pg. 14 of the 3rd Edition) to enter the waveforms for the simulation. To enter the value, right click on the node go to “Value – Count Value”. In each case, under the “Timing” tab, the “Count Every” field should be entered as 100ns (see Figure 11). Once you have completed this, save your vector waveform file and again it is easiest to accept the default name on the file which is “lab1”.

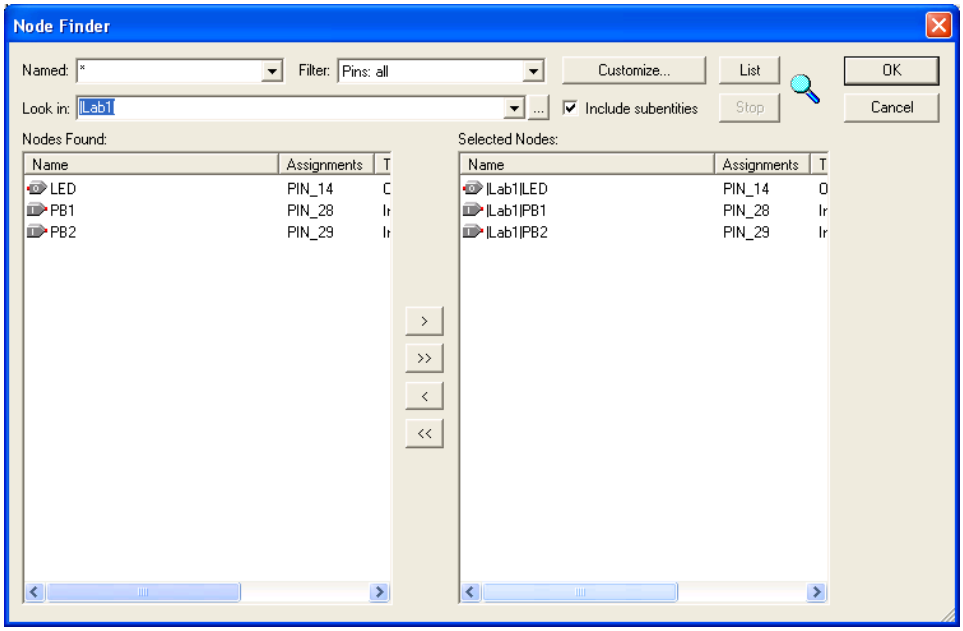

Figure 10. Node finder for simulation setup

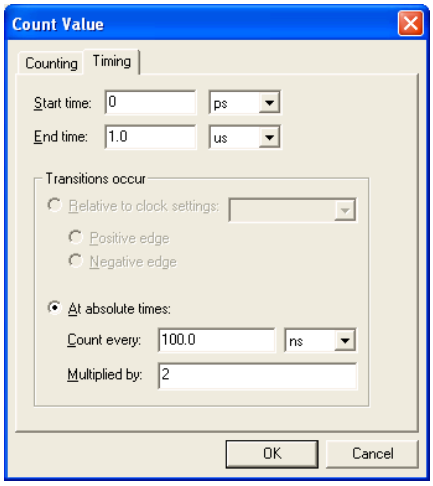

Figure 11. Simulation Values – Timing Tab

We are now ready to simulate the output. The software will take the inputs which we have entered and simulate what the output will be over the same time range. Note that this is **NOT** synthesis as we have not even touched the hardware yet. We are doing everything in software for now.

Click on the  button and this brings up the simulation screen. Ensure that the software has selected the correct .vwf file and if it has then just click on the "Start" button to begin the simulation.

By clicking on "Report" or "Open", you will see what the simulated output is. Print a copy of this for inclusion in your report.

E. Download the program to the board

You can follow the instructions found on pages 22 to 24 in the textbook. Choose "Tools – Programmer" and click on "Hardware Setup". Select the USB-BLASTER [USB-0] and click OK and then in the main screen click on "Auto Detect". This should detect that the device we are using is an EP2C35F672C6 device. If it does not then this can be manually selected.

Now add a file to the programmer by clicking on "Add file" and locate your lab1.sof file (or whichever name you called the file). Make sure that you **delete any other file** so that the only file in the list is yours. Then press "Start" and the circuit is synthesized on the CPLD. We now have a hardware implementation of our design and can play with the push button switches and the LED. So, try out each combination of the push buttons and note whether the LED lights up or not in each case.

F. Timing and Routing

We will now look at timing and routing by following the instructions in sections 1.l3 and 1,14 1.9 found on pages 38 to 40 in the text.

G. VHDL Implementation

We will now implement the same circuit but instead of using a schematic we will use VHDL to describe the circuit.

First of all close the project that you have been working on up to this moment by using "File – Close Project".

Notes:

- Open a new file under "File – Open – VHDL File". This gives us a text editor to use. We will follow the instructions in the book on pages 29-33 The  button

will be very useful for inserting entity, architecture statements etc. Save the file in a different directory and you will be prompted to create a new project which you should do.

- We must successfully compile the file before any assignments can be made.

4. Lab Exercises

- Enter the function $F(A,B,C) = A\overline{B} + BC$ and simulate its performance for every possible input. Are there any hazards in this circuit?
- Complete exercises 3, 9 and 10, pg. 42-43. Note: for changes to the floorplan you can drag and drop the used logic block (colored square). Then turn on the fan in and fan out and you will see that is redirected to this block. In the assignment editor, you will now see that the new block is in use. Recompile so that this block is used in fitting and the timing analysis will show the new results. We will go over this in class.

5. Report

- Follow the report guidelines in writing up your report.
- Include documentation of your circuit designs and show that they worked as intended (simulation results). You should embed these figures in your write-up rather than attaching the results – make sure to caption all figures appropriately and describe the results in the figures.
- Include answers to each of the lab exercises and have a separate subsection for each question in the results section

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