# *ECE318 Laboratory #2*
## *Lab Date: Jan. 22th  Report Due: Jan. 29th*

# Introduction to Modelsim and K-Map Revision

## 1. Introduction

This lab will provide an introduction to the ModelSim VHDL simulator and give you more experience with the Quartus VHDL synthesis tool. It will also provide a review of combinational circuit design and reinforce circuit delay properties discussed in class. A decoder for a 7-segment display will be designed using K-maps and then simulated with both ModelSim and Quartus. Finally, the logic will be synthesized with Quartus. This should reinforce the difference between simulation and synthesis.

## 2. Prelab

Reread chapter 2 of "Rapid Prototyping of Digital Systems – A Tutorial Approach". Pay particular attention to the definition of the pins for the 7-segment display and the switches. Use SW1, SW2, and SW3 and HEX0.

Design a decoder that decodes the input switches SW3-SW1 to the patterns on a 7-segment LED display as shown in Table 1. Use Figure 2.3 in the lab manual to define the individual LED output segment names. From the last lab, **recall that the LEDs are active low, so they light up when they receive a 0**. Use K-maps to minimize the design. Your final design should be the equations needed for a dataflow VHDL model of the decoder.

| SW3 | SW2 | SW1 | LED Display |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

**Table 1. LED Display for given switch values**

# 3. Procedure

We will first use Modelsim which is purely a simulation tool. The tool is fairly similar to Quartus and so the detail provided below is not expansive.

## 3.1. ModelSim Simulation

### a) Create a project

Projects are meant to help you organize a large design, but they are necessary even for small designs.

Select "File – New – Project" to create a new project. This opens the "Create Project" dialog (as shown in Figure 1) where you can specify a project name, location, and default library name. You can generally leave the "Default Library Name" set to "work". If you specify the project location to a directory which does not exist you will be prompted to create this directory. For example, the "Project Name" can be set to Lab2 and the "Project Location" to "H:\ECE318\Lab2". Make sure to save all files on your thumb drive.

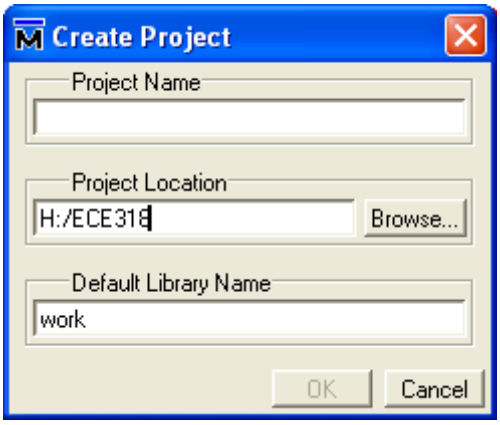


**Figure 1. Create Project dialog**

### b) Create the VHDL file

1. Assume all gates have a 1 ns delay and calculate a maximum delay for each output. Use this in your model. Create decoder7.vhd VHDL file using your favorite text editor (make sure to add the suffix **.vhd**). After you have created the file, you can add the file to your project by right clicking in the "Project" window and then choosing "Add to Project – Existing File". Alternatively, you can use the Modelsim text editor by choosing "File – New – Source – VHDL". (Use the

Windows XP file properties to use your editor of choice to open all VHDL files.) Store it in the project directory.

2. You need to ensure that Modelsim knows that the file is a VHDL file. Right click on the file to bring up the Properties dialog box as shown in Figure 2.

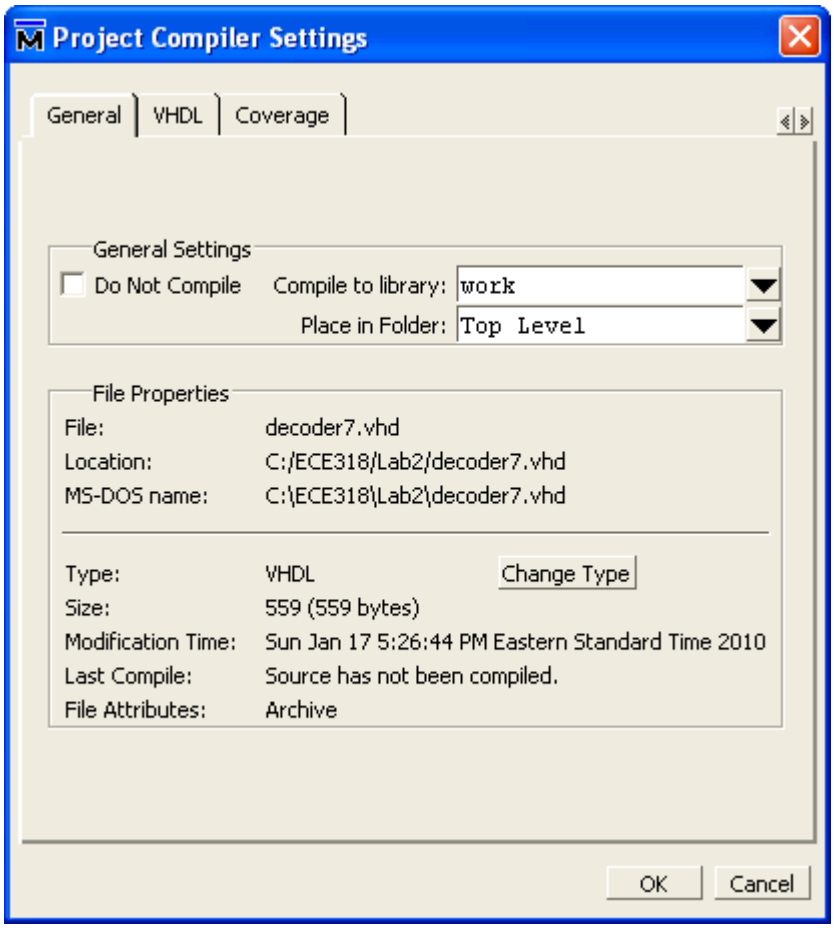


**Figure 2. File Properties dialog**

Click on the Change Type button and set the "File Type" to VHDL as shown in Figure 3 (if it is not already of this type).

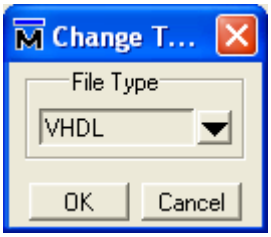


**Figure 3. Change Type dialog box**

### c) Compile the file

1. Click on "compile" button. If the compile is successful, go to the next step. Otherwise, choose "Compile – Compile-Report" to view the errors and fix them. By clicking on each error you can obtain more information about the error.
2. Click on the "Library" tab in the workspace window and notice that there is a "work" library listed. Expand work to see your compiled design entity and architecture. The "work" library is where designs are compiled to by default.

### d) Simulate the file

1. Download the following testbench file: decoder_tb.vhd to your project directory and add it to your project by selecting "File – Add to Project – Existing File" which brings up the dialog in Figure 4.

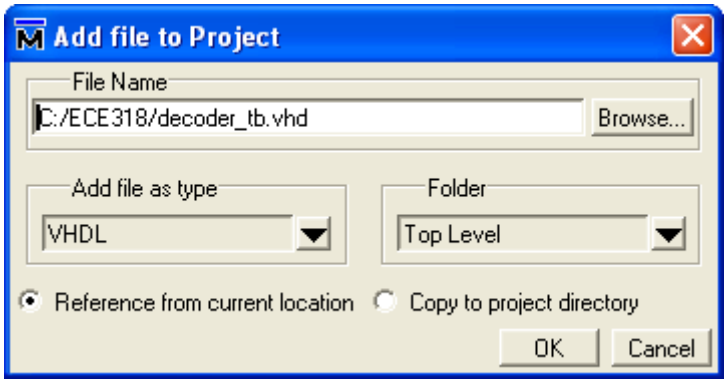


**Figure 4. Add file to Project dialog**

2. Select the file and use View-Properties to set it to compile using 2002 syntax as seen in Figure 5

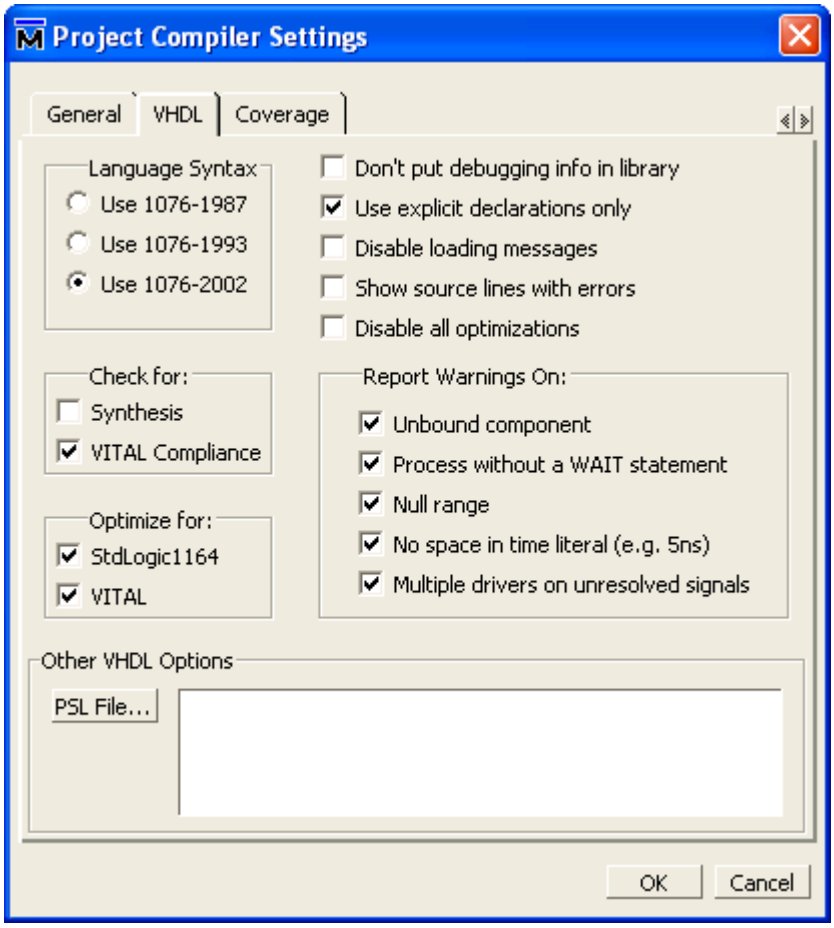


**Figure 5. Compiler Settings dialog**

3. Compile the testbench file. **Fix any errors that might occur due to inconsistencies with the component declaration (i.e., the component declaration must match exactly your decoder7.vhd entity – all the port names have to be exactly the same).**
4. On the library tab, highlight the decoder_tb compiled file, right click and choose "Simulate". A new tab named "sim" appears in the Workspace pane. Click on "View" and select the "Objects" and "Wave" panes. You can undock a window and move it around by clicking on one of the symbols in the top right hand corner of the pane.
5. In the objects window "Select all" and "drag and drop" the objects on the Wave pane.
6. Simulate the design for 1 microsecond by typing "run 1 us" in the Transcript pane to run the simulation. The results will be plotted in the Wave Pane.
7. Check the results and verify that they are correct. Measure some of the delays in the simulation. Do they match the delays you modeled? Make sure that you take print outs or screenshots of your results so that you can include these in your report.

## 3.2. Quartus Simulation and Synthesis

Since we completed a very similar procedure last week, the details in this lab are kept to a minimum.

**a) Compilation and Simulation**

Open your decoder7.vhd file in Quartus. Create a project (make sure you target the correct the Cyclone II family and the EP2C35F672C6 device), compile, and simulate the design. You will have to create an input waveform in the waveform editor. Measure the delays from the waveform or using the delay analysis tool. How do the delays compare to what you modeled in VHDL? Why?

**b) Synthesis**

Use the "Assignment Editor" to assign signals from your design to pin numbers. Pin numbers for the switches and display are given in Table 2.4, page 35 of your manual.

Once you have assigned the device and pins, recompile your design and download the programming file to the DE2 board. You may want to refer back to the details in last week's lab if you get stuck.

**c) Testing the Design in Hardware**

We now have the design implemented in hardware and can play with the switches to make sure that our design works. Change the switches on the board and verify that the LEDs are correct for the switch inputs. Demonstrate your working circuit to your lab instructor.

# 4. Report

Be sure to include all design information in your report including

- K-maps and equations for the outputs
- Delay estimates used in VHDL model
- Simulation results and discussion of delays measured in ModelSim and Quartus.
- Description of board testing results.

Winter 2013