Union College
ECE363
Fall 2017
Assignment 3

Reading Due Thursday October 19, 2017

1. Read Professor Buma's notes 6. Pay particular attention to using Darlington transistors and single supply op-amps.
2. Read through Professor Buma's notes 7 and 8. Read in the textbook about differential amplifiers starting on page 628, and T model starting on page 303.

The following problems are due Thursday October 23, 2014

A. DC Analysis of Long-Tail Pair

Problem 1: (Adapted from Problem 17-4 in the textbook) Many differential amplifiers are intended for single-ended output (the collector of Q_2). Therefore, the collector resistor of Q_1 is not necessary. Assume $\beta = 100$ for both transistors.

a) What is the tail current in Fig. 1? Express your answer in mA.
b) What is r_e' for each transistor?
c) What is the quiescent collector voltage of Q_2?

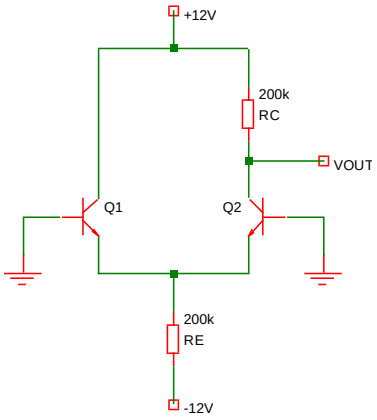

Fig. 1: Problem 1

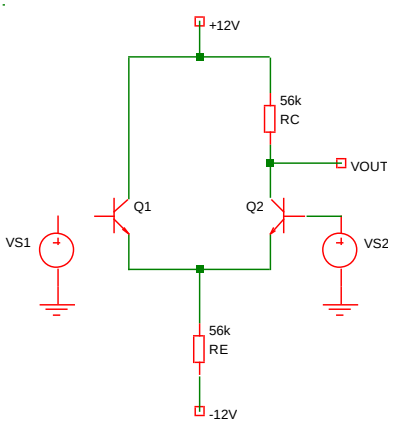

Fig. 2: Problem 2

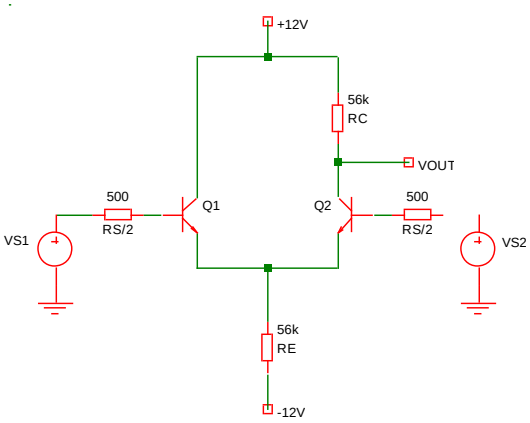

Fig. 3: Problem 3

B. Small Signal Analysis of Long-Tail Pair

Problem 2: Consider a differential input $\Delta V_{IN} = V_{S1}-V_{S2}$.Assume both transistors have $\beta = 100$, $V_{BE} = 0.7V$, and $V_{CE,SAT} = 0.3V$.

a) What is the differential gain $\Delta V_{OUT}/V_{IN}$ in Fig. 2?
b) If $V_{S1} = -V_{S2} = 10$ mV, what is $V_{OUT} = V_{CQ} + \Delta V_{OUT}$?
c) What is the largest ΔV_{IN} that does not produce a clipped output?

Problem 3: Any realistic input has a non-zero source resistance R_S. In Fig. 3, R_S is split evenly between V_{S1} and V_{S2}. This means the differential input $\Delta V_{IN} = V_{B1}-V_{B2}$ is smaller than the signal source input $\Delta V_S = V_{S1} – V_{S2}$. Assume $\beta = 100$ and $V_{BE} = 0.7V$ for both transistors.

a) What is the differential gain $\Delta V_{OUT}/\Delta V_{IN}$?
b) What is the input impedance R_{IN} of the amplifier? Express your answer in kΩ.
c) What is the ratio $\Delta V_{IN}/\Delta V_S$? Hint: Remember that R_{IN} and R_S form a voltage divider.
d) Compute ΔV_{OUT} if $V_{S1} = +5$ mV and $V_{S2} = -5$mV.

C. Long-Tail Pair Design

Problem 4: Design a differential amplifier with $A_d \geq 100$ and $R_{IN} \geq 50$ kΩ. The power supplies are $V_{CC} = V_{EE} = 12$ V. Assume both transistors have $\beta = 100$ and $V_{BE} = 0.7V$.

a) Compute the necessary tail current I_T.
b) Choose the proper value for R_E (standard 5% resistor).
c) Based on your choice of R_E, compute your actual I_T and input impedance R_{IN}.
d) Choose the proper value for R_C (standard 5% resistor).
e) Based on your chosen values for R_E and R_C, compute the actual gain $A_d = \Delta V_{OUT}/\Delta V_{IN}$ and quiescent output voltage of your amplifier.
f) What is the overall signal gain V_{OUT}/V_S? Keep in mind that the 4.7 kΩ resistance appears at both inputs.

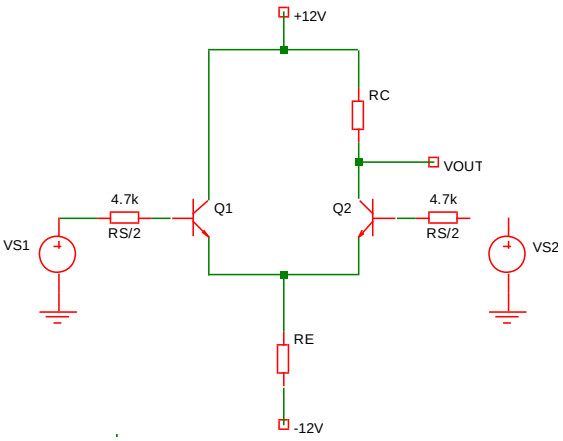

Fig. 4: Problem 4

Problem 5: Design a differential amplifier with $A_d \geq 100$ and $R_{IN} \geq 20$ kΩ. The power supplies are $V_{CC} = V_{EE} = 10$ V. Assume both transistors have $\beta = 40$ and $V_{BE} = 0.72V$.

a) Compute the necessary tail current I_T.
b) Choose the proper value for R_E (standard 5% resistor).
c) Based on your choice of R_E, compute your actual I_T and input impedance R_{IN}.
d) Choose the proper value for R_C (standard 5% resistor).
e) Based on your chosen values for R_E and R_C, compute the actual gain $A_d = \Delta V_{OUT}/\Delta V_{IN}$ and quiescent output voltage of your amplifier.

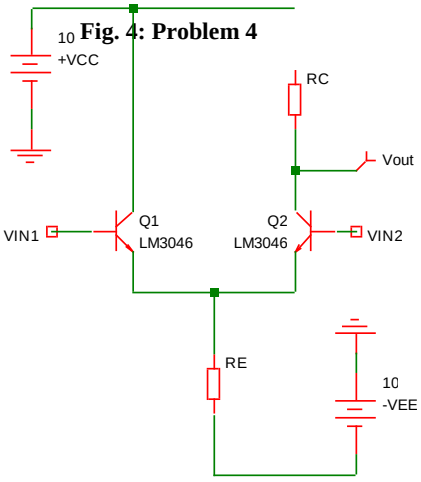

Fig. 5: Problem 5

D. Common Mode Rejection Ratio

Problem 6: Analyze the long-tail pair shown in Fig. 6. Assume both transistors have $\beta = 100$ and $V_{BE} = 0.7V$.

a) Compute the input impedance R_{IN}.
b) Compute the differential gain A_d.
c) Compute the common mode gain A_{CM}.
d) Compute the CMRR.

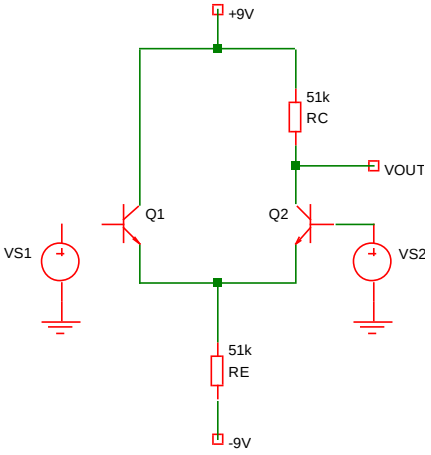

Fig. 6: Problem 6

Problem 7: Compute the CMRR of your amplifier designs from Problem 4 and 5.

E. Transistor Current Source

Problem 8: Consider a simple transistor current source. Technically, this circuit is a "current sink", because it pulls current from the load. But the name "current source" is usually used anyway. Assume $\beta = 100$, $V_{BE} = 0.7V$, and $V_A = 120$ V for the transistor.

a) Compute the zener current (the 1N4735A is a 6.2V zener).
b) Compute the current that is pulled through the load.
c) Compute the output impedance R_{OUT} of the current source.

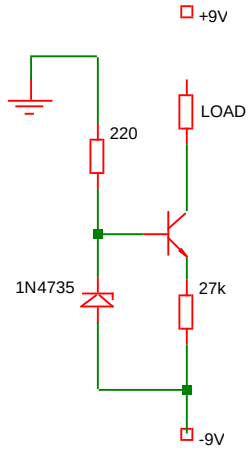

Fig. 7: Problem 8

F. Differential Amplifier with Current Source Biasing

Problem 9: Design a current source to bias your differential amplifier design from Problem 4. This current source will replace the tail resistor R_E in your original design. Use a 5.1V zener and standard 5% resistors for R_B and R. Assume $\beta = 100$, $V_{BE} = 0.7V$, and $V_A = 120$ V for the current source transistor. Compute the CMRR of this improved differential amplifier. It should be considerably better than your result in Problem 7.

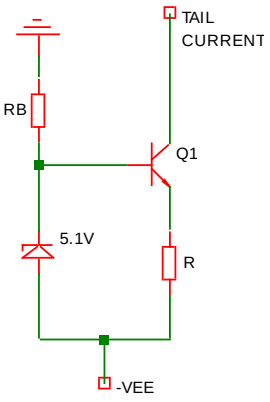

Fig. 8: Problem 9

Problem 10: Design a current source to bias your differential amplifier design from Problem 5. This current source will replace the tail resistor R_E in your original design. Use three

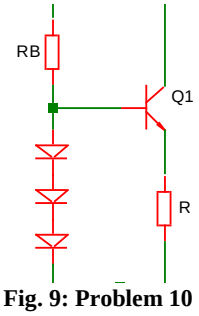

Fig. 9: Problem 10

diodes (V_F = 0.7V) to bias the transistor and standard 5% resistors for R_B and R. Assume β = 100, V_{BE} = 0.7V, and V_A = 120 V for the current source transistor. Compute the CMRR of this improved differential amplifier. It should be considerably better than your result in Problem 7.